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| **Project Group Title:** | | **F3-16: FPGA & HMC Tools & Architectures for RSC** |
| **Faculty Investigators:** | | Dr. Herman Lam, Dr. Alan D. George |
| **Group Leaders:** | | Abhijeet Lawande |
| **Brief Summary:** | | |
| 2015 was a breakout year for reconfigurable supercomputing (RSC), with key players in high-performance and data-center computing making significant investment into reconfigurable computing (RC); including IBM, Microsoft, Micron, and Intel. During the past year we have observed the rapid integration of RC technologies into the conventional computing space. Key examples include Microsoft’s Catapult system, IBM’s Coherent Accelerator Processor Interface (CAPI), and Micron’s Hybrid Memory Cube (HMC). Leading and riding this wave of resurgence, F3-16 aims to explore and advance key technologies for RSC through four projects. Project 1 will focus on the exploration and evaluation of high-level synthesis (HLS) tools and direct interconnects to utilize CAPI and the POWER architecture efficiently for RSC. Project 2 will explore and develop novel reconfigurable interconnects using Novo-G# to accelerate communication-intensive large-scale apps. Project 3 will create a research vehicle to study processing-in-memory concepts using FPGA and HMC devices. Project 4 will evaluate optimization and productivity issues with HLS tools targeted towards firmware development for the Large Hadron Collider at CERN. | | |
| **Project 1:** | Multi-device Acceleration on POWER Architecture | |
| **Students:** | Kenneth Hill, Siddharth Sharma | |
| **Progress, Roadblocks, and Outcomes in Past Month:**   * Preparing SC16 demo to highlight design options for CAPI and FPGAs: RTL (VHDL/Verilog)+PSL, OpenCL, OpenCL+RTL, OpenCL+Networking (via OpenCL pipes) * Completed STAC-A2 max-up-to-now payoff functionality on Nallatech 510T platform w/ dual Arria10 FPGAs   **Goals and Plans for Next Month:**   * Add routing capabilities to OpenCL+Networking Board Support Package (BSP) for CAPI * Functionally verify all STAC-A2 financial benchmark components (Monte Carlo, Longstaff-Schwartz, etc.) using Altera OpenCL emulator and deploy design on Nallatech 510T platform w/ dual Arria10 FPGAs | | |
| **Project 2:** | Reconfigurable Interconnects for Novo-G# | |
| **Students:** | AbhijeetLawande | |
| **Progress, Roadblocks, and Outcomes in Past Month:**   * Implemented 3D FFT and LBM using reconfigurable topology on 16 Novo-G# nodes to verify simulation accuracy; Less than 9% error in simulation observed; Reconfigurable interconnect hardware overhead measured at 8% or less * Completed survey of cluster OS’s for use in Novo-G upgrade & division; Stacki being considered as a potential replacement   **Goals and Plans for Next Month:**   * Document Novo-G# AOCL support with reconfigurable networks & associated VisualSim models in preparation for code release * Improve Novo-G# software support and scheduling in preparation for use by external users | | |
| **Project 3:** | Custom Memory Cube (CMC) | |
| **Students:** | Yu Zou, Vinayak Deshpande, Suvrat Tedia | |
| **Progress, Roadblocks, and Outcomes in Past Month:**   * Modified Convey's PERFMON code to isolate memory accesses for measuring key perf. parameters; Obtained NDA from Micron * Developed initial performance measurement and modeling methods for blocking-memory-access DRE operations using Design Option 3 (view buffer in HMC)   **Goals and Plans for Next Month:**   * Conduct experiments to measure performance of blocking-memory-access DRE operations * Explore performance measurement and modeling methods for overlapping-memory-access DRE ops | | |
| **Project 4:** | CMS Endcap L-1 Muon Trigger | |
| **Students:** | Abhinandan Jyothishwara , Yiheng Xia, Nikhil Ghanathe | |
| **Progress, Roadblocks, and Outcomes in Past Month:**   * Solved integration-latency issue for Module 2; Completed integration of first three modules * Integrating and performing hardware verification of Modules 4 & 5; found one mismatch in Module 4, missing RTL logic in Module 5; Achieving automation of hardware verification upon integration of each module   **Goals and Plans for Next Month:**   * Debug mismatch in hardware verification of Module 4 and integration issue in Module 5 * Continue integration of other modules to complete integration & verification process | | |